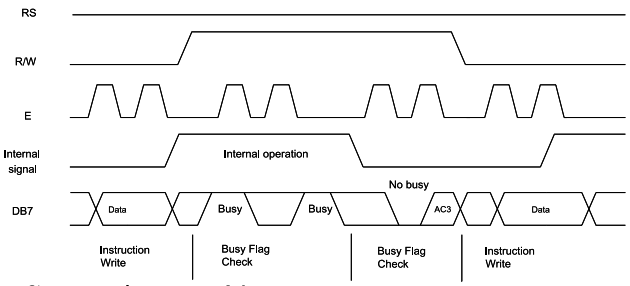
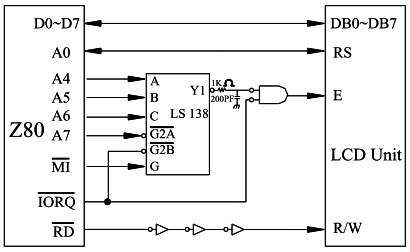
INTERFACE TO MPU
(GRAPHIC TYPE MODULE)

LCD GROUP

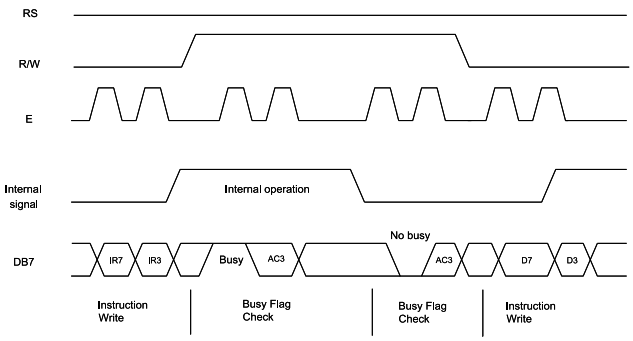
Interface to 8-bit MPU



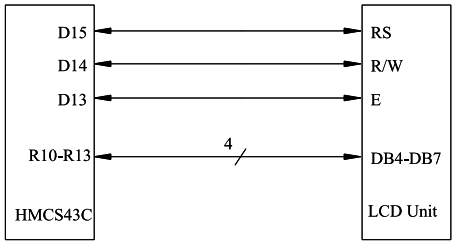
Connection to Z80



INTERFACE TO MPU



Connection to HMCS43C



INITIALIZING BY INSTRUCTIONS

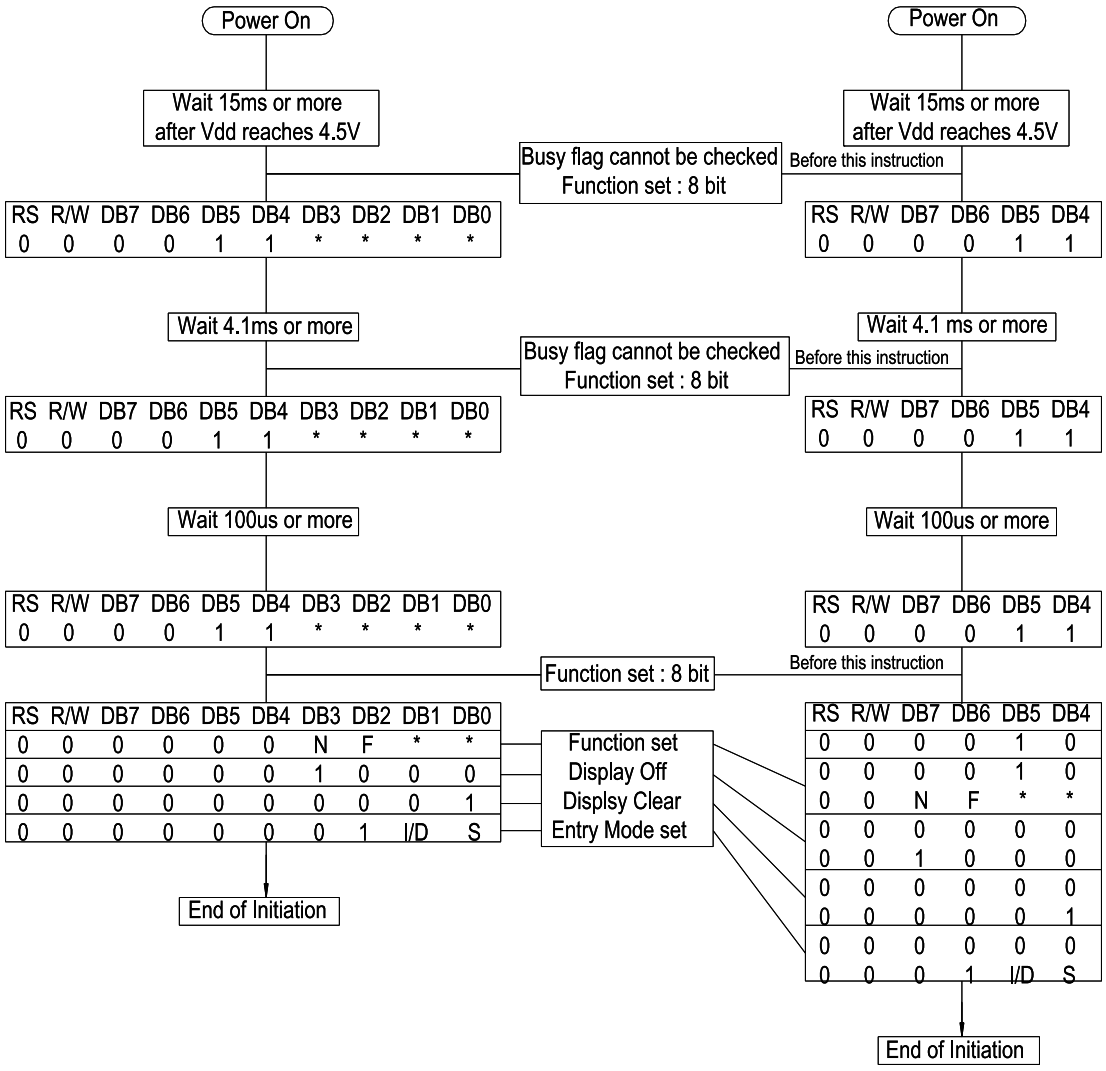
(CHARACTER TYPE MODULE)

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instruction is required , or use the following procedure for initialization .

Instructions

1) 8 Bit interface

2) 4 Bit interface



- Busy flag be check after following instruction are completed . If busy flag is not checked, the waitting time between instructions should be longer than the execution time of these instructions.

LCD GROUP

INSTRUCTIONS
(CHARACTER TYPE MODULE)

Instruction	Code										Description	Execution Time(max) (When fcp or fosc is 250 KHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clear entire display and sets DD RAM address 0 in address counter	1.64ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 in address counter. Also returns display being shifted to original position. DD RAM contents remain unchanged.	1.64ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display. These operations are performed during data write and read .	40us
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of entire display(D),Cursor ON/OFF(C),and blink of cursor position character(B).	40us
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor & shifts display without changing DD RAM contents.	40us
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display Lines(L) and character fonts(F).	40us
Set CG RAM Address	0	0	0	1	ACG						Set CG RAM address. CG RAM data is sent and received after this setting.	40us
Set DD RAM Address	0	0	1	ADD							Set DD RAM address. CG RAM data is sent and received after this setting.	40us
Read Busy Flag and Address	0	1	BF	AC							Reads Busy flag(BF)indicating internal operation is being performed and reads address counter contents.	0us
Write Data To CG or DD Ram	1	0	Write Data								Write data into DD RAM or CG RAM	40us
Read Data To CG or DD Ram	1	1	Read Data								Read data into DD RAM or CG RAM	40us
	1/D = 1 : Increment 1/D = 0 : Decrement S = 1 : Accompanies display shift S/C= 1:Display shift S/C= 0 : Cursor move R/L=1 : Shift to the right R/L= 0 : Shift to the left DL= 1: 8 bits , DL= 0: 4 bits N = 1: 2 lines , N=0:5 x 7 dots FB= 1 : Internally operating FB= 0: Can accept instruction or data										DD RAM : Display data RAM CG RAM : Character generator RAM ACG : CG RAM address ADD : DD RAM address: Corresponds to cursor address AC: Address counter used for both DD and CG RAM address.	Execution time Changes when Frequency changes Example: When fcp or fosc is 270 KHz: 40usx250/270=37us

LCD GROUP

INSTRUCTIONS
(GRAPHC TYPE MODULE)

Class	Command	Code												Command Description	Number of Read Bytes
		RD	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0	Hex		
System Control	SYSTEM SET	1	0	1	0	1	0	0	0	0	0	0	40	Initialize device and display	8
	SLEEP IN	1	0	1	0	1	0	1	0	0	1	1	53	Enter standby mode	0
Display Control	DISPLAY ON/OFF	1	0	1	0	1	0	1	1	0	0	D	58 59	Enable and disable display and display flashing(D=0; Display OFF,D=1;Display ON)	1
	SCROLL	1	0	1	0	1	0	0	0	1	0	0	44	Set display start address and display regions	10
	CSRFORM	1	0	1	0	1	0	1	1	1	0	1	5D	Set cursor tyoe	2
	CGRAM ADR	1	0	1	0	1	0	1	1	1	0	0	5C	Set start address of character generator RAM	2
	CSRDIR	1	0	1	0	1	0	0	1	1	C2	C1	4C TO 4F	Set direction of Cursor Movement C C2 C1 Shift Direction 4CH 0 0 Right 4DH 0 1 Left 4EH 1 0 Up 4FH 1 1 Down	0
	HDOT SCR	1	0	1	0	1	0	1	1	0	1	0	5A	Set horizontal scroll position	1
	OVLAY	1	0	1	0	1	0	1	1	0	1	1	5B	Set display overlay format	1
Drawing Control	CSRW	1	0	1	0	1	0	0	0	1	1	0	46	Set cursor address	2
	CSRR	1	0	1	0	1	0	0	0	1	1	1	47	Read cursor assress	2
Memory Control	MWRITE	1	0	1	0	1	0	0	0	0	1	0	42	Write to display memory	-
	MREAD	1	0	1	0	1	0	0	0	0	1	1	43	Read from display memory	-

[Notes]

1. In general, internal registers of the SED 1330F are modified as each command parameter is input. However, the microprocessor does not have set all the parameters of a command and may send a new command before all parameters have been input.
The internal regiters for the parameters that have been input will have been changed but the remaining parameter registers are unchaged.
2byte parameters (where two bytes are treated as 1 data item) are handled as follows:
a.CSRW, CSRR:E ach byte is processored individually. The microprocessor may read or write just the low byte of the cursor address.
b.SYSTEM SET,SCROLL,CGRAM ADR: Both parameter bytes are processed together.
if the command is changed after half of the parameter has been input, the single byte is ignored.